Figure 5 is a flowchart of a SPICE to Verilog translation process. The translation process 500 begins with SPICE netlist 502 that is opened and read in at step 504. Table 1 below lists an example SPICE file input and Table 2 below lists an example Verilog file output. At step 506, instantiations of the heading ".SUBCKT" are translated to "module". A circuit name, and input and output signal names, may follow the ".SUBCKT" heading. The circuit name may be identified as the first word following ".SUBCKT" and may be utilized as the module name. Input and output signal names follow the circuit name and may be may be employed in the Verilog output file. For example, the ".SUBCKT INV_CHAIN Z A" line of table 1 may be employed to generate the "module INV_CHAIN (Z, A)" entry listed in table 2. Retaining the circuit name and input and output signal names allows simplified association of the SPICE input file with the Verilog output file. Alternately, new circuit and signal names may be introduced in the translation process. At step 508, ".ENDS" statements are translated to "endmodule". At step 510, "x" elements are translated to Verilog format. The 'x' elements may comprise an instance name, signal nodes, and a circuit element descriptor. For example, the "XINV3 2 3 INV" line listed in table 1 may be translated to the "INV INV3 (.Z(3), .A(2)):" line listed in table 2. The translation of instance names ("XINV1" to "INV1" in the above example), may employ simple truncation of a leading "x" in element names, or may employ renaming. Renaming may be total or in part and may employ a lookup table, an algorithm, or rules to define the instance name. Advantageously, the present invention allows the hierarchy of the SPICE design and signal name associations to be maintained. The signal node names of the SPICE file may be employed to define wires in Verilog, and to specify signal connections to Verilog circuit elements. As may be observed in table 2, the signal nodes listed in table 1 are defined as wires. The circuit element descriptor may be translated to Verilog syntax. In the examples of tables 1 and 2, INV is used for both SPICE and Verilog syntax. At step 512, discrete circuit elements, such as resistors, capacitors, transistors, and inductors, for example, are removed. At step 514, the modified file is written out to produce Verilog structured netlist 516.